

CLAIM AMENDMENTS

Please amend Claims 1, 3, 5, 7, 9, 11, 13, 15, 17-23, 25, and 27, and cancel Claims 2, 4, 6, 8, 10, 12, 14, 16, 24 and 26 as follows:

1. (Currently Amended) An image processing apparatus for sensing a continuous multiple-chip-extending image and for generating data representing the image, comprising:

a plurality of sensor chips connected to one another and positioned relative to each other so as to collectively receive the continuous multiple-chip-extending image without an insensitive region therebetween caused by circuit wiring, each sensor chip including a first pixel row and a second pixel row, which are formed on the same semiconductor chip, the first pixel row having a plurality of pixels arranged in a main scanning direction, and the second pixel row having a plurality of pixels shifted along the main scanning direction with respect to the first pixel row;

a first output line, connected to each first pixel row of each of said plurality of sensor chips to receive first pixel signals from each first pixel row of each of said plurality of sensor chips; and

a second output line, connected to each second pixel row of each of said plurality of sensor chips to receive second pixel signals from each second pixel row of each of said plurality of sensor chips.

2. (Cancelled)

3. (Currently Amended) An image processing apparatus for sensing a continuous multiple-chip-extending image and for generating data representing the image, comprising:

a plurality of sensor chips connected to one another and positioned relative to each other so as to collectively receive the continuous multiple-chip-extending image without an insensitive region therebetween caused by circuit wiring, each including a first pixel row and a second pixel row, which are formed on the same semiconductor chip, the first pixel row having a plurality of pixels arranged in a main scanning direction, and the second pixel row having a plurality of pixels shifted along the main scanning direction with respect to the first pixel row;

a first output line provided outside said plurality of sensor chips, to which a signal from ~~the~~ said first pixel row in each of ~~the~~ said plurality of sensor chips is read; and

a second output line provided outside said plurality of sensor chips, to which a signal from ~~the~~ said second pixel row in each of ~~the~~ said plurality of sensor chips is read;

a driving circuit, which drives said plurality of sensor chips to sequentially output signals to ~~the~~ said first output line and ~~the~~ said second output line; and

a combining circuit provided outside said plurality of sensor chips and connected to said first and second output lines to receive signals from said first and second output lines from the first and second pixel rows of each of said plurality of sensor chips, which selectively outputs the signals from ~~the~~ said first output line and ~~the~~ said second output line, wherein said combining circuit is common to said plurality of sensor chips.

4. (Cancelled)

5. (Currently Amended) An image processing apparatus according to Claim 3, further comprising an analog-to-digital converting circuit arranged to receive an output from said combining circuit,

wherein the signals from ~~the~~ said first pixel row and ~~the~~ said second pixel row of each of said plurality of sensor chips are selectively outputted by said combining circuit as a resulting signal, and the resulting signal is converted into a digital signal by said analog-to-digital converting circuit.

6. (Cancelled)

7. (Currently Amended) An image processing apparatus according to Claim 3, further comprising an analog-to-digital converting circuit,

wherein the signals from ~~the~~ said first pixel row and ~~the~~ said second pixel row of each of said plurality of sensor chips are converted into digital signals by said analog-to-digital converting circuit, and the ~~resulting~~ digital signals are selectively outputted.

8. (Cancelled)

9. (Currently Amended) An image processing apparatus according to Claim 3, further comprising:

a first reference level adjusting circuit, configured to receive from said first output line the first pixel signals from each of said plurality of sensor chips and to adjust ~~which adjusts~~ the reference level of the first pixel signals from each of said plurality of sensor chips ~~signal from the first pixel row~~; and

a second reference level adjusting circuit, configured to receive from said second output line the second pixel signals from each of said plurality of sensor chips and to adjust ~~which adjusts~~ the reference level of the second pixel signals from each of said plurality of sensor chips ~~signal from the second pixel row~~,

wherein said first reference level adjusting circuit and said second reference level adjusting circuit are provided before said combining circuit.

10. (Cancelled)

11. (Currently Amended) An image processing apparatus for sensing a continuous multiple-chip-extending image and for generating and transmitting data representing the continuous image, comprising:

a plurality of sensor chips connected to one another and whose imaging regions are positioned relative to each other so as to collectively receive the continuous multiple-chip-extending image without an insensitive region therebetween caused by circuit wiring, each of said plurality of sensor chips including:

an imaging region; ~~region~~, a

a first readout circuit; ~~circuit~~, a

a second readout circuit; ~~circuit~~, a

a first output ~~unit; and unit, and a~~
a second output unit,
wherein said plurality of sensor chips ~~which~~ are formed on the same
semiconductor chip,
wherein each ~~the~~ imaging region of each of said plurality of sensor
chips has ~~having~~ a first imaging region and a second imaging region, each having a
plurality of pixels arranged in ~~the~~ a main scanning direction,
wherein said ~~the~~ first readout circuit of each of said plurality of sensor
chips for is configured to selectively read ~~reading~~ a signal from ~~the~~ each of said plurality of
pixels in ~~the~~ said first imaging region of the sensor chip to which said first readout circuit
belongs,
wherein said ~~the~~ second readout circuit of each of said plurality of
sensor chips is configured to ~~for~~ selectively read ~~reading~~ a signal from ~~the~~ each of said
plurality of pixels in ~~the~~ said second imaging region of the sensor chip to which said
second readout circuit belongs,
wherein said ~~the~~ first output unit of each of said plurality of sensor
chips is configured to output ~~for outputting~~ the signal read ~~from~~ by said first readout circuit
of the sensor chip to which said first output unit belongs, and
wherein said ~~the~~ second output unit of each of said plurality of sensor
chips is configured to output ~~for outputting~~ the signal read ~~from~~ by said second readout
circuit of the sensor chip to which said second output unit belongs;
a first output line provided outside said plurality of sensor chips, to
which signals ~~a signal~~ from ~~the~~ each first pixel row in each of ~~the~~ said plurality of sensor

chips is read through each of said first readout circuits and each of said first output units of said plurality of sensor chips; and

a second output line provided outside said plurality of sensor chips, to which a ~~signal~~ signals from ~~the~~ each second pixel row in each of ~~the~~ said plurality of sensor chips is read through each of said second readout circuits and each of said second output units of said plurality of sensor chips;

a driving circuit, which drives said plurality of sensor chips to sequentially output signals to ~~the~~ said first output line and ~~the~~ said second output line from said first output unit and said second output unit, respectively; and

a combining circuit provided outside said plurality of sensor chips, which selectively outputs the signals from ~~the~~ said first output line and ~~the~~ said second output line, wherein said combining circuit is common to said plurality of sensor chips.

12. (Cancelled)

13. (Currently Amended) An image processing apparatus according to Claim 11, further comprising an analog-to-digital converting circuit arranged to receive an output of said combining circuit,

wherein the signals from said the first imaging region and said second imaging region of each of said plurality of sensor chips ~~pixel row and the second pixel row~~ are selectively outputted by said combining circuit, and the resulting signal is converted into a digital signal by said analog-to-digital converting circuit.

14. (Cancelled)

15. (Currently Amended) An image processing apparatus according to Claim 11, further comprising an analog-to-digital converting circuit,

wherein the signals from said the first imaging region and said second imaging region pixel row and the second pixel row are converted into digital signals by said analog-to-digital converting circuit, and the ~~resulting~~ digital signals are selectively outputted.

16. (Cancelled)

17. (Currently Amended) An image processing apparatus according to Claim 11, further comprising:

a first reference level adjusting circuit, configured to receive from said first output line the signals from each of said plurality of pixels of each first imaging region of said plurality of sensor chips and to adjust ~~which adjusts~~ the reference level of the signals from each of said plurality of pixels of each first imaging region of said plurality of sensor chips ~~signal from the first pixel row~~; and

a second reference level adjusting circuit, configured to receive from said second output line the signals from each of said plurality of pixels of each second imaging region of said plurality of sensor chips and to adjust ~~which adjusts~~ the reference level of the signals from each of said plurality of pixels of each second imaging region of said plurality of sensor chips ~~signal from the second pixel row~~,

wherein said first reference level adjusting circuit and said second reference level adjusting circuit are provided before said combining circuit.

18. (Currently Amended) An image processing apparatus according to Claim 1, wherein the second pixel row is positioned to be offset ~~shifted~~ by half the pixel pitch in the main scanning direction with respect to the first pixel row.

19. (Currently Amended) An image processing apparatus according to Claim 1, wherein the first pixel and the last pixel in each of ~~the~~ said plurality of sensor chips are arranged in different pixel rows.

20. (Currently Amended) An image processing apparatus according to Claim 1, wherein the number of pixels in the first pixel row is equal to the number of pixels in the second pixel row in each of ~~the~~ said plurality of sensor chips.

21. (Currently Amended) An image processing apparatus according to Claim 1, wherein the first pixels in all of ~~the~~ said plurality of sensor chips are positioned in the same pixel row.

22. (Currently Amended) An image processing apparatus according to Claim 1, wherein the distance in a sub-scanning direction between the center of the first pixel row and the center of the second pixel row in each of said plurality of sensor chips is an integer multiple of the pixel pitch in the main scanning direction.

23. (Currently Amended) An image processing apparatus according to Claim 1, further comprising:

a light source, positioned to emit ~~which emits~~ light to illuminate an original document; and

a lens array, configured and positioned to guide ~~which guides~~ light reflected from the original document to said plurality of sensor chips.

24. (Cancelled)

25. (Currently Amended) An image processing apparatus according to Claim 3, further comprising:

a light source, positioned to emit ~~which emits~~ light to illuminate an original document; and

a lens array, configured and positioned to guide ~~which guides~~ light reflected from the original document to said plurality of sensor chips.

26. (Cancelled)

27. (Currently Amended) An image processing apparatus according to Claim 11, further comprising:

a light source, positioned to emit ~~which emits~~ light to illuminate an original document; and

a lens array, configured and positioned to guide ~~which guides~~ light
reflected from the original document to said plurality of sensor chips.